METHOD AND DEVICE TO MAINTAIN SYNCHRONIZATION TRACKING IN TDD WIRELESS COMMUNICATION

FIELD OF THE INVENTION

The invention relates to a method and device to maintain synchronization tracking, in particular, to a method and device in TDD Wireless Communication System.

BACKGROUND OF THE INVENTION

TD-SCDMA is a 3G standard adopted by ITU. It takes advantages of TDMA and synchronous CDMA, provides high spectrum efficiency and service flexibility. In TD-SCDMA UE system, it is very important that UE is synchronized to the received signal from Node-B. In general, signal synchronization can be divided into two stages: initial synchronization and synchronization tracking. The base of synchronization is on chip level. Every chip in Node-B is shaped into an ISI-free waveform by using shaping filter, shown in Figure 1. Denote the waveform function of RRC filter as f(t). In UE system, to acquire the maximum SINRN, UE should sample at the peak of the chip waveform, corresponding to time=0 in Figure 1. In TD-SCDMA, there are two sub-frames in each radio frame, which is of 10ms length. The sub-frame format is shown in Figure 2. In a sub-frame, there are seven common time slots and two special time slots. The two special time slots include DwPTS and UpPTS. In Figure 3, the structure of common time slot is shown. There are two data parts in one time slot, and in the middle of the two data parts, there is a midamble part. Midamble is used to estimate the radio multi-path and is also quite important in maintaining the downlink synchronization.

After having acquired the initial synchronization of the downlink signal, UE enters into the stage of keeping the synchronization. Because UE does not know the

exact time offset information between local timer and the downlink signal from Node-B, traditionally X-times sampling rate is used, here X is an integer larger than 1, i.e. 2, 4 or even 8. Then UE uses RRC filter to filter the sample stream. The filter output will shape auto-correlation waveform of SYNC-DL. The highest peak corresponds to the most likely synchronization point. Using the method, the synchronization time error will be within [-T_c/2X, T_c/2X]. "Early/late gate" is a commonly seem implementation according to above theory. Another commonly used synchronization method is "τ dithering loop".

Because high value of sample multiple X raises the speed requirement for A/D converter, bigger buffer size and computation complexity are required. And then those will raise the cost of the hardware system and the consumption of the A/D conversion. So in general, smaller sample multiple is better, but if sample multiple is too small, the synchronization precision will decrease, so from above X is set as 4 often.

SUMMARY OF THE INVENTION

The invention want to resolve the technical problem of providing a new interlaced sampling method to sample the midamble part in TD-SCDMA time slot, and in this way, when sampling multiple is 1, the system still keeps goodish synchronization tracking performance. When sampling multiple is 1, namely, the real offset within [-T_c/2, T_c/2], rough synchronization has acquired.

The technical project of the invention includes the following steps:

a、 Divide midamble into two parts, then detect the first one and the second one of the midamble respectively;

b、 Do auto-correlation operation of above two parts and the corresponding part of local midamble to obtain two peaks;

c、 compare two peaks;

d、 Decide advances or retards of local timer base on the compared results.

The said sample time point for detecting midamble is:

1. when $353 \leqslant n \leqslant 496$, if n is even, the sample time point is $(n-\Omega)T_c$;

2. when $353 \leqslant n \leqslant 496$, if n is odd, the sample time point is $(n+\Omega)T_c$;

Here, Ω must be a smaller value, because if Ω is too bigger, the auto-correlation peak shown in Fig 8. will decrease, which is disadvantage to channel detecting. The principle to select Ω value is that Ω is random value less than 1/4. In this way, the time difference between $(n+\Omega)T_c$ and $(n-\Omega)T_c$ is less than half of the chip period, midamble {m1, m2, m3,... m144} is divided into odd part {m1, m3, m5, ... m143} and even part {m2, m4, m6,... m144}. Detect the odd part and the even part of the midamble by using match filter and obtain two peaks, then compare the two peaks amplitude. If the latter is higher than the former, advance the local timer by ΩT_c; by contraries, if the former is higher than the latter, advance the timer by $-\Omega T_c$; the said midamble is also downlink synchronization sequence.

Thereinafter, take 16th midamble as example. When use other signal sequence, the result is same. As odd part and even part has same auto-correlation peak and the peak is the half of the auto-correlation peak of entire signal sequence, assume the sampling offset is τ. Under adopting normal sampling method, the peak of midamble auto-correlation is direct proportional to $f(\tau)$, however, under adopting the interlaced-sampling method of the invention, the peak of midamble auto-correlation is proportional to $[f(\tau+\Omega)+f(\tau-\Omega)]/2$, so the normalized error of channel detecting induced by interlaced-sampling will be about:

$$2f(\tau)/[f(\tau+\Omega)+f(\tau-\Omega)], \quad -T_c/2<\tau<T_c/2, \qquad (1)$$

As can be seen, the both are nearly the same except that the peak amplitude of the latter one is a little lower than the former one. Compared with the normal method, the new interlaced-sampling method will only harm SNR of channel detecting very slightly using midamble. By using this new method, the sample frequency can be decreased to only one time of the chip rate and TD-SCDMA can still maintain the ability to track the downlink synchronization. In this way, it can be allowed to adopt cheaper A/D converter and to reduce the buffer size greatly. The tracking error can be mostly within $[-T_c/16, T_c/16]$, which is same as the error when adopting normal method and X=8.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

Fig 1. is RRC Shaping Filter Response.

Fig 2. is the structure of sub-frame.

Fig 3. is the structure of time slot.

Fig 4. is the error of channel estimation with interlaced midamble.

Fig 5. is the sampling point offset of current data parts.

Fig 6. is a concrete mode of carrying out the invention implemented in the device of downlink synchronization tracking in TDD wireless communication system.

Fig 7. is concrete mode of carrying out the invention implemented in the triggering device in the device shown in Fig 6.

DETAILED DESCRIPTION OF THE INVENTION

In initial designing, Ω is set as 1/16. By controlling the triggering pulse to A/D converter, the sampling time points for all the 864 chips in a time slot are

1. when $1 \leqslant n \leqslant 352$, the sampling time point is nT_c;

2. when $353 \leqslant n \leqslant 496$, if n is even, the sampling time point is nT_c;

3. when $353 \leqslant n \leqslant 496$, if n is odd, the sampling time point is nT_c;

4. when $497 \leqslant n \leqslant 864$, the sampling time point is nT_c.

The said n is chip location, the said Ω is random value less than 1/4, the said T_c is chip period. In the example, the said midamble is midamble. The midamble {m1, m2, m3, ... m144} is divided into odd part {m1, m3, m5, ... m143} and even part {m2, m4, m6, ... m144}. Detect the odd part and the even part of midamble using match filter and obtain two peaks, then compare the two peaks amplitude. If the latter (even part) is higher than the former (odd part), advance the local timer by Tc/16; by contraries, if the former is higher than the latter, advance the timer by $-T_c/16$; said signals sequence can be midamble, also downlink synchronization sequence.

According to above method, because the peak of the auto-correlation of odd part (and even part) has only half the amplitude of that of entire midamble, in noisy environment, the SNR of the odd part (and even part) is 3 dB lower than that of entire midamble. This may lead to more errors in comparison of auto-correlation peak amplitude of odd part and even part. Next, a example will be taken to explain the feasibility of the invention method.

Assume that one vehicle runs at 120km/hr and moves 0.167m in every sub-frame time (5ms). When the distance between UE and Node-B is changed because of movement, UE should advance/retard local downlink timer by $T_c/16$ (chip rate is 1.28M, T_c=781ns). In period time $T_c/16$, wireless wave can transmit 14.5m distances at 300,000km/s, which means: if UE really need advance/retard local downlink timer because of movement, it can make decision after comparing auto-correlation peak of odd part and even part in as many as [14.65/0.167] = 87 sub-frames. There are at least two downlink time slots in one sub-frame, so in 87

sub-frames there are at least 174 usable midamble to be decided. This makes a nearly error-free decision.

According to above deduction, there can be as many as 174 comparison results. If more than $[174(1+\Delta)/2]=N_T$ results are positive, the local timer advances Tc/16; on the contrary, local timer retards $T_c/16$. Here $[\cdot]$ means the integer no greater than. If there are not more than N_T positive or negative comparison results, local timer remains unchanged. Here Δ is a protection margin which is used to avoid unnecessary dithering of the local timer (in the following mathematical analysis, Δ is set as 0.1).

When the vehicle speed is lower than 120km/hr, UE can compare auto-correlation peaks of more than 174 odd and even parts before making decision. This will lead to better performance.

As can be seen in Fig 5, Δ marks odd sampling point, ∇ marks even sampling point. Assume that the sampling point of current data part has offset T_{offset}, $-T_c/2< T_{offset} <T_c/2$, then correct tracking will be advance local timer by $\pm$Tc/16 towards the correct direction. So correct tracking is the important precondition of implementing the invention.

In the analysis, maybe selected parameters are not best (such as value of Δ, the interlaced offset Ω and the adjustment step $T_c/16$, etc.), but in real environment they can be tuned to perform better.

As can be seen in Fig 6, there is a device for downlink synchronization tracking in TDD wireless system, which includes the following connected in turn:

A/D converter 1 to convert analog signals to data signals;

Distributor 2 to divide midamble into odd part and even part;

Two FIFO memories 3 to temporarily save the signals from Distributor 2;

Dot product 4 to do auto-correlation operation to the odd part and even part of the midamble from memories 3 and the respectively corresponding part of the local midamble;

Compare Decision 5 to compare the auto-correlation peaks of the both parts;

Local timer 6 to decide advances or retards according to decision results.

The output signals of said local timer 6 triggers A/D converter 1 through triggering mechanism 7.

As can be seen in Fig 7, there is a triggering mechanism 7 for downlink synchronization tracking in TDD wireless communication. The triggering mechanism 7 includes: the first counter 71 to provide pulse indicating, umpty switches, the second counter 72 to provide chip location indicating.

The said switches turn on and turn off according to the pulse indication of the first counter 71 and the location indication of the second counter 72. The said first counter is hexadecimal. The said switches include the following three switches: he first switch 73, the second switch 74 and the third switch 75. When pulse indication is 15, chip location indication is 353～496 and is even, the first switch 73 closes; when pulse indication is 1, chip location indication is 353～496 and is odd, the second switch 74 closes; when pulse indication is 0, chip location indication is 1～352. 497～864 the third switch 75 closes.

The invention does not be restricted to above method and device. The device shown in Fig 6 and Fig 7 are also implemented adopting software partly, such as the said midamble can be also divided into two parts using other way. So all the technical changes known by the person skilled in the field should fall into the protective scope of the invention.